FIG. 1

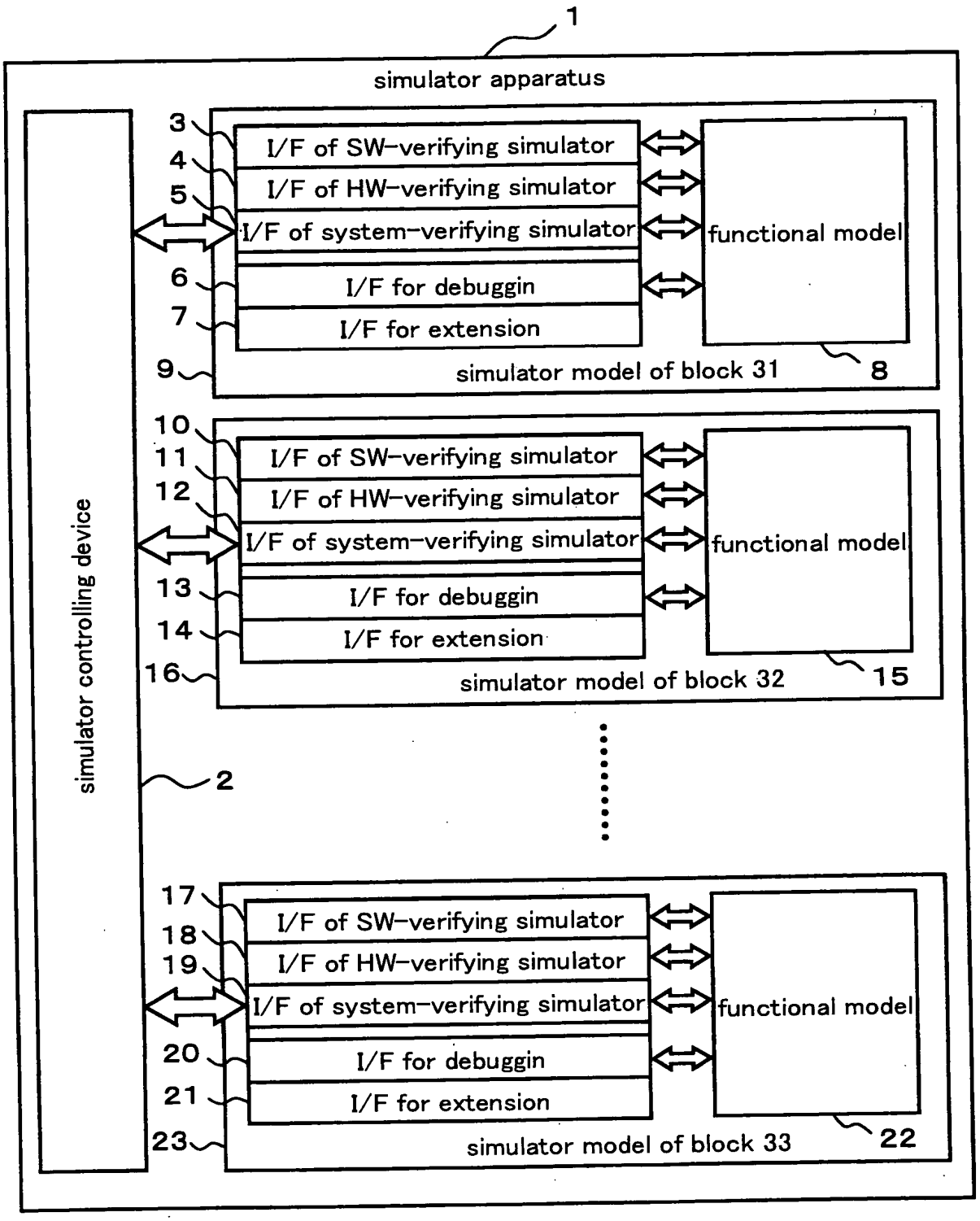

1
simulator apparatus
simulator controlling device
2
3
4
5
6
7
9
I/F of SW-verifying simulator
I/F of HW-verifying simulator
I/F of system-verifying simulator
I/F for debuggin
I/F for extension
functional model
8
simulator model of block 31
10
11
12
13
14
16
I/F of SW-verifying simulator
I/F of HW-verifying simulator
I/F of system-verifying simulator
I/F for debuggin
I/F for extension
functional model
15
simulator model of block 32
17
18
19
20
21
23
I/F of SW-verifying simulator
I/F of HW-verifying simulator
I/F of system-verifying simulator
I/F for debuggin
I/F for extension
functional model
22
simulator model of block 33

FIG. 2

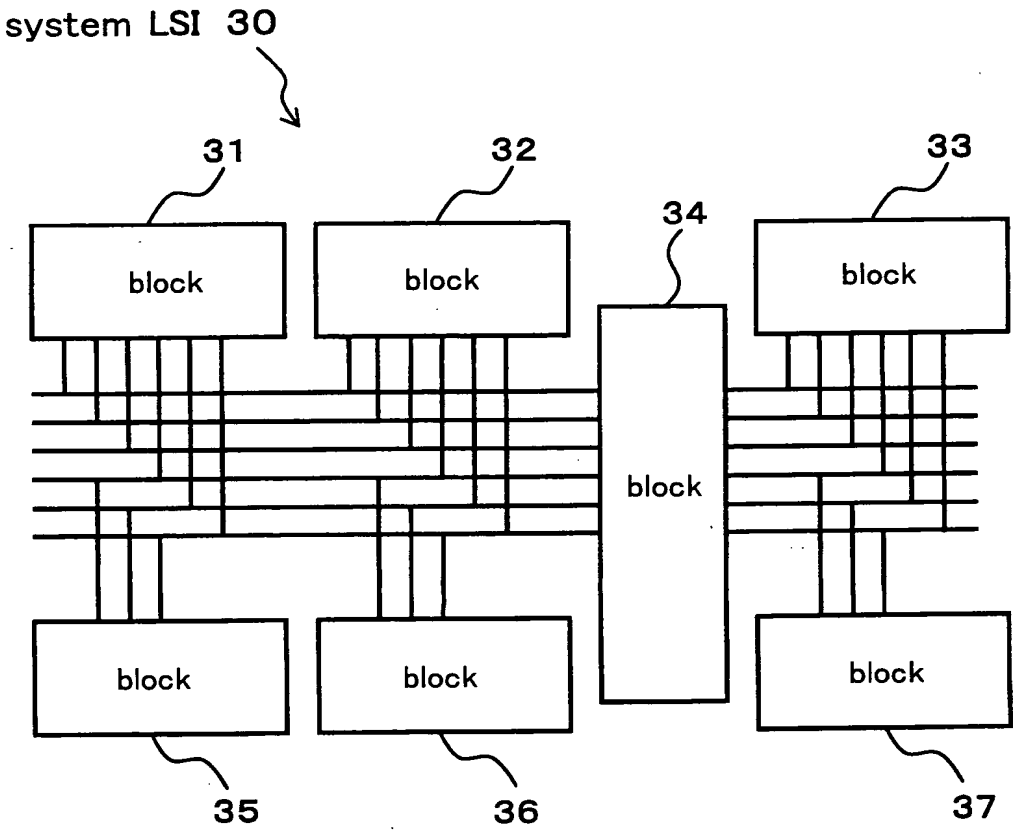

system LSI 30
31
32
33
34
block
block
block
block
block
block
block
block
35
36
37

FIG. 3

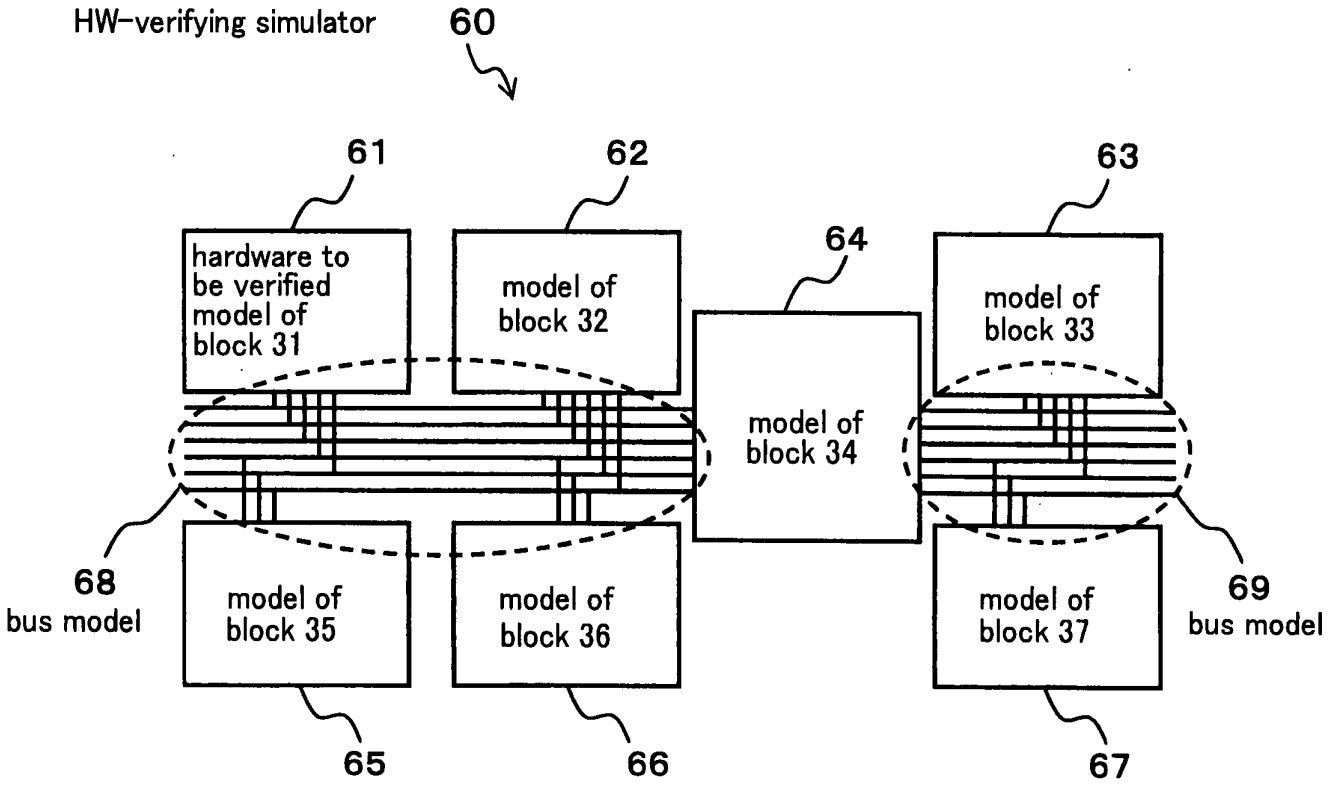

HW-verifying simulator
60
61
62
63
64
hardware to be verified model of block 31
model of block 32
model of block 33
model of block 34
68
bus model
model of block 35
model of block 36
model of block 37
69
bus model
65
66
67

FIG. 4A

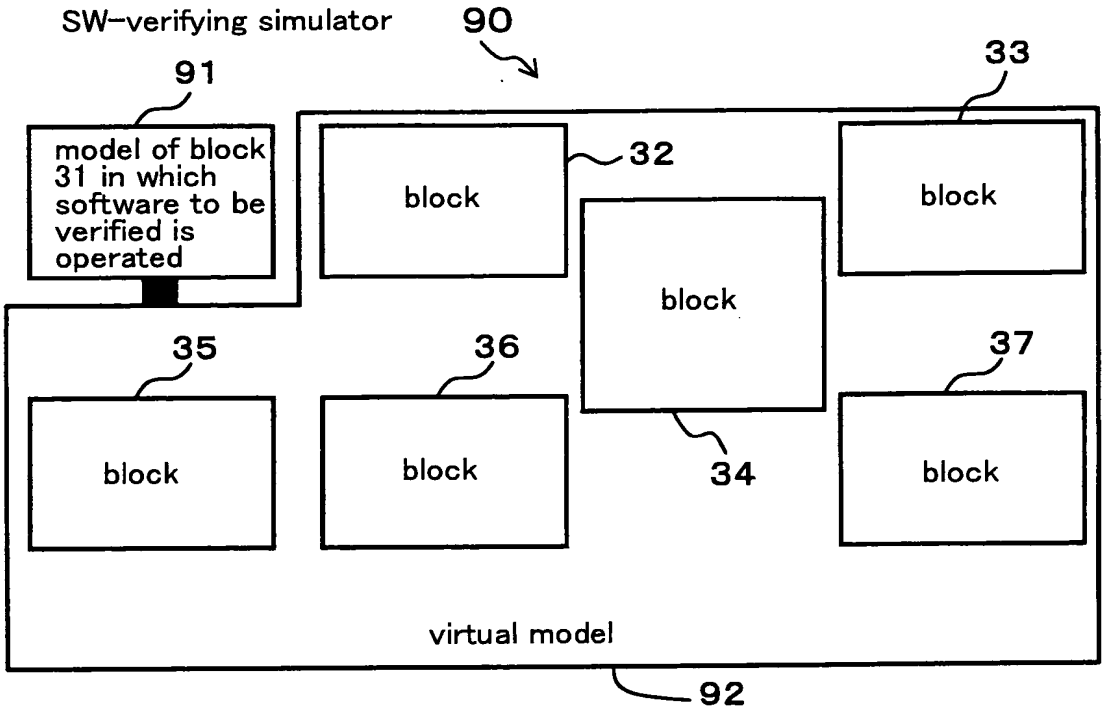

SW-verifying simulator
90
91
33
model of block 31 in which software to be verified is operated
block
32
block
block
35
36
37
block
block
34
block
virtual model
92

FIG. 4B

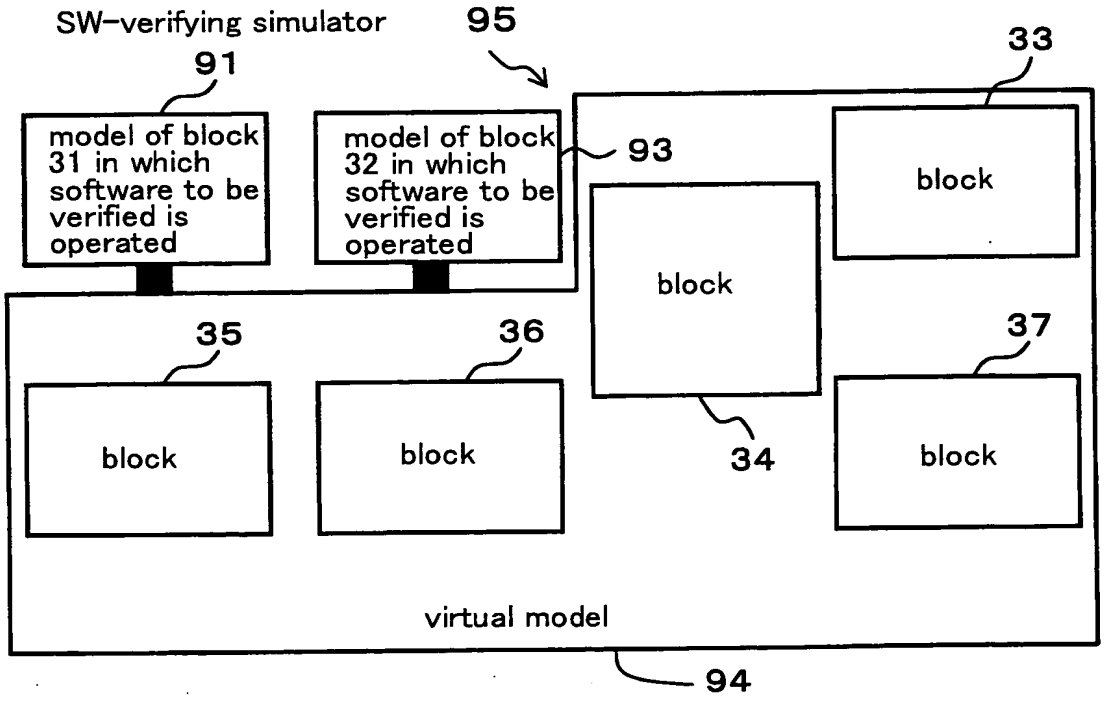

SW-verifying simulator
95
91
33
model of block 31 in which software to be verified is operated
model of block 32 in which software to be verified is operated
93
block
block
35
36
37
block
block
34
block
virtual model
94

FIG. 5

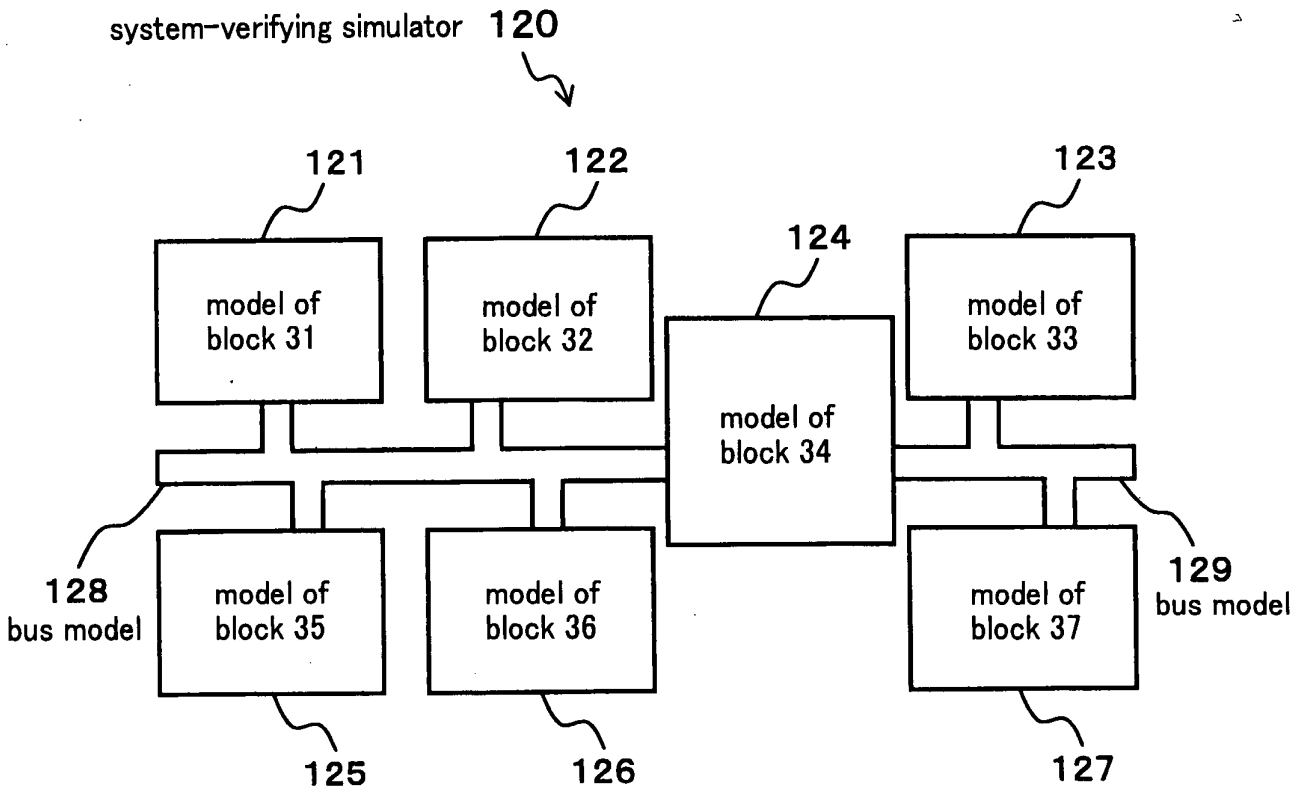

system-verifying simulator 120
121
122
123
124
model of block 31
model of block 32
model of block 33
model of block 34
128
bus model
model of block 35
model of block 36
model of block 37
129
bus model
125
126
127

FIG. 6

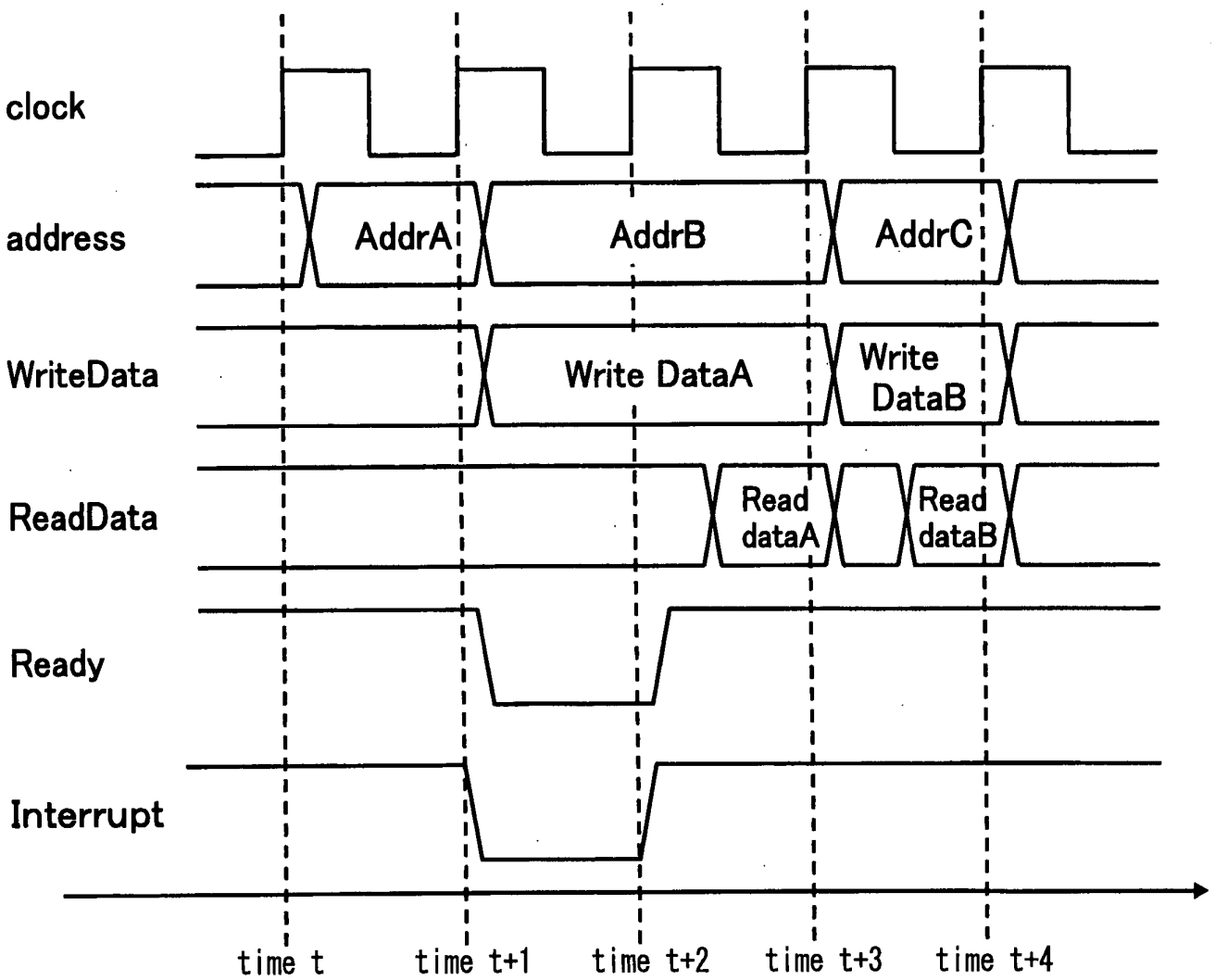

clock
address
AddrA
AddrB
AddrC
WriteData
Write DataA
Write DataB
ReadData
Read dataA
Read dataB
Ready
Interrupt
time t
time t+1
time t+2
time t+3
time t+4

FIG. 7

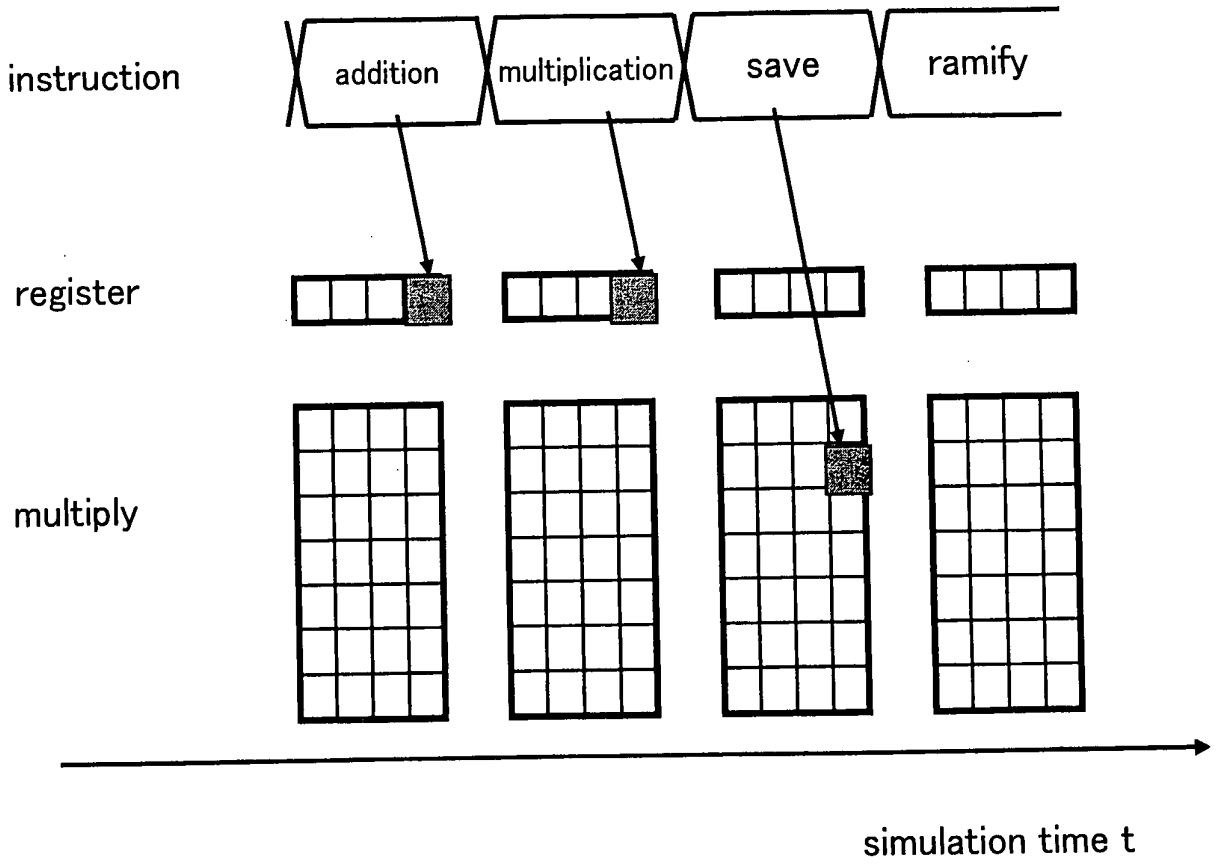

instruction
addition
multiplication
save
ramify
register
multiply
simulation time t

FIG. 8

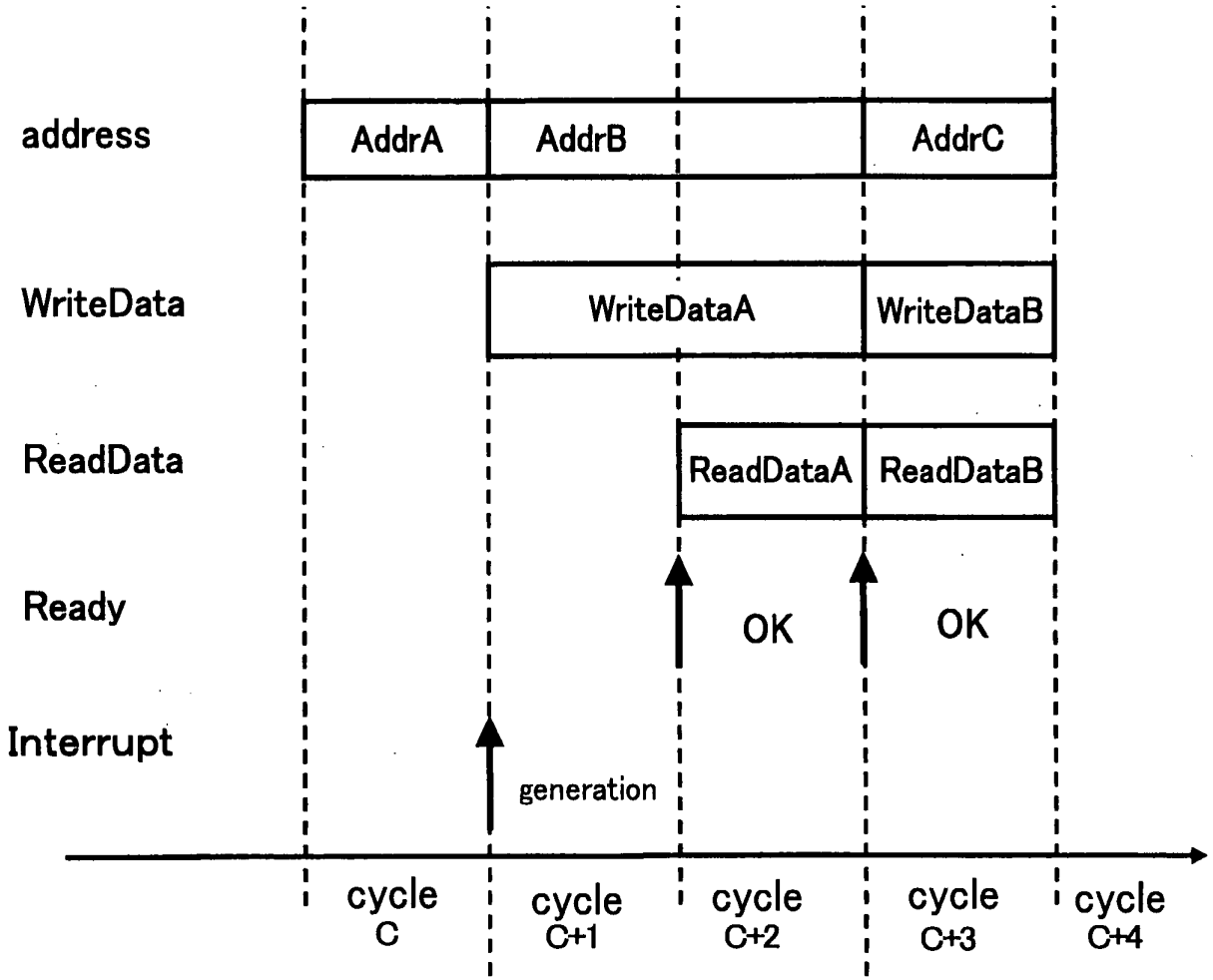

address
AddrA
AddrB
AddrC
WriteData
WriteDataA
WriteDataB
ReadData
ReadDataA
ReadDataB
Ready
OK
OK
Interrupt
generation
cycle C
cycle C+1
cycle C+2
cycle C+3
cycle C+4

FIG. 9

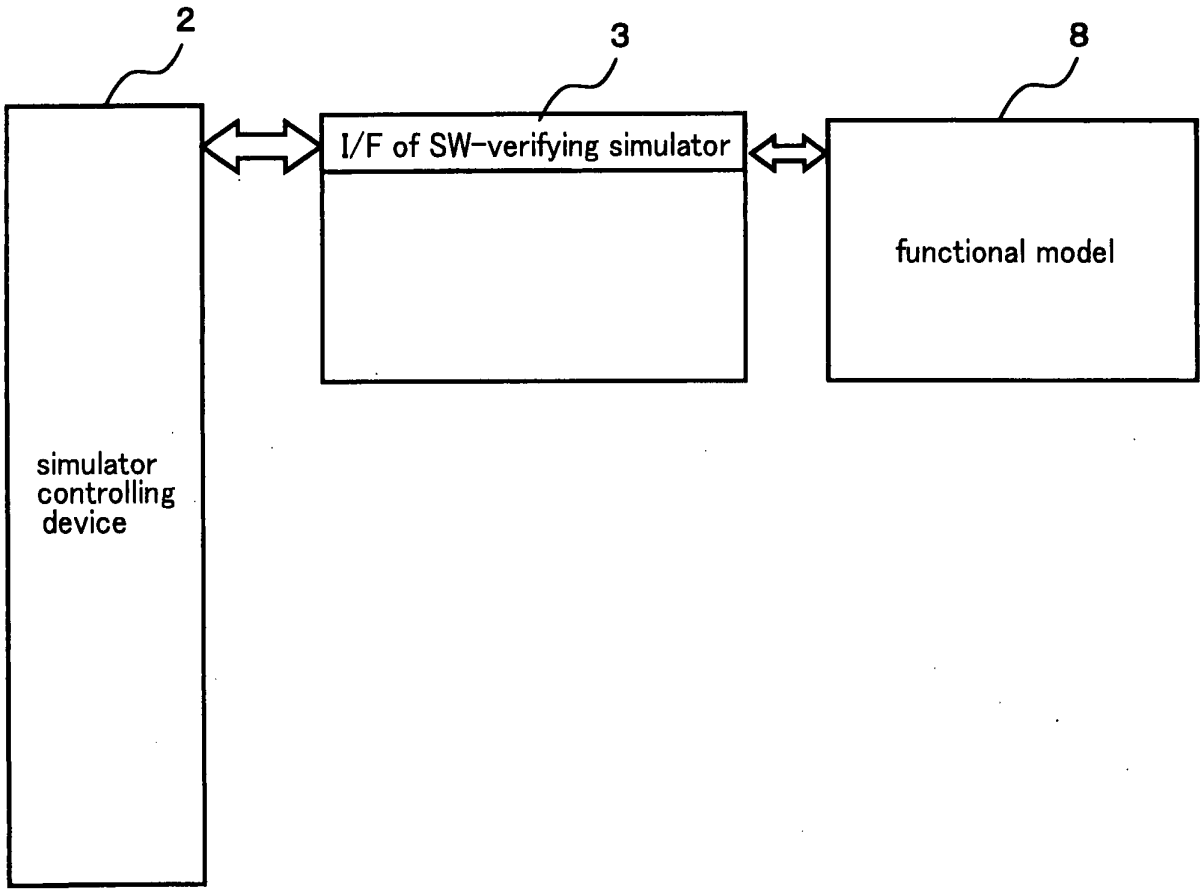

2
3
8
I/F of SW-verifying simulator
functional model
simulator controlling device

FIG. 10
PRIOR ART

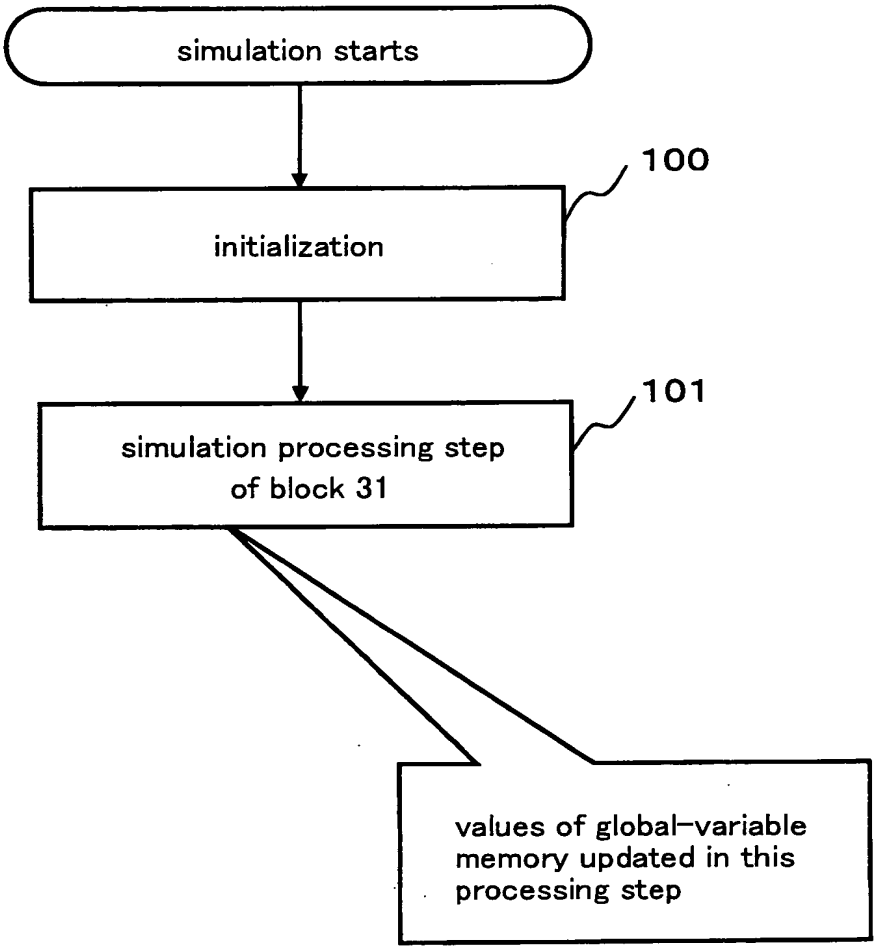


FIG. 11

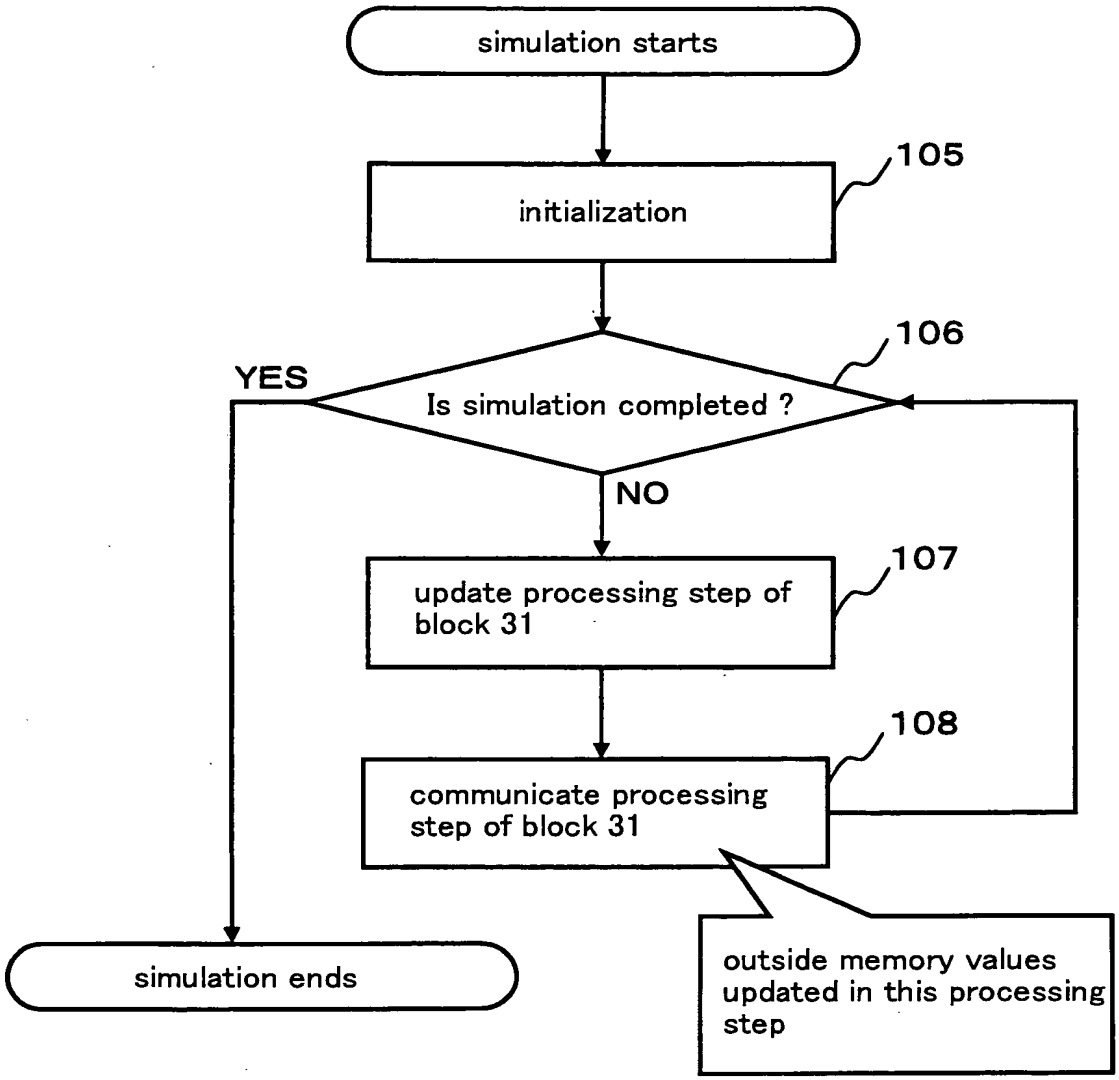

simulation starts
initialization
105
Is simulation completed ?
106
YES
NO
update processing step of block 31
107
communicate processing step of block 31
108
simulation ends
outside memory values updated in this processing step

FIG. 12

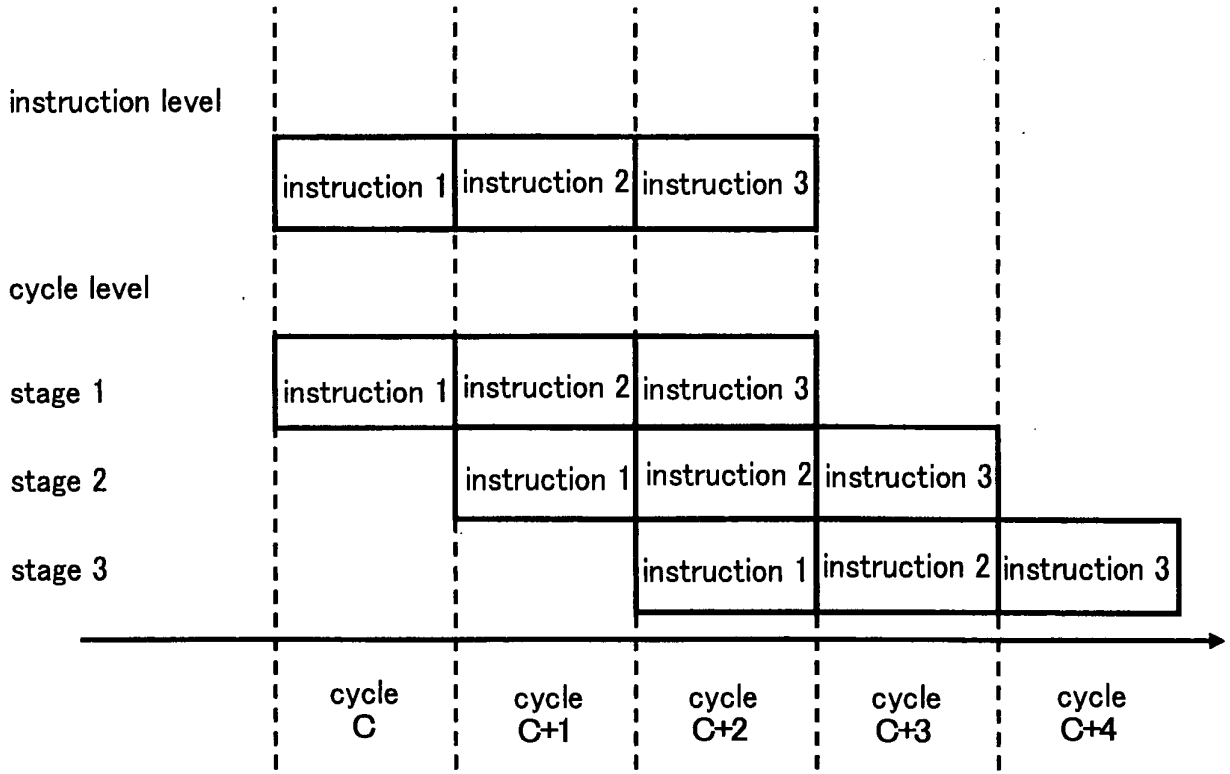

instruction level
instruction 1
instruction 2
instruction 3
cycle level
stage 1
instruction 1
instruction 2
instruction 3
stage 2
instruction 1
instruction 2
instruction 3
stage 3
instruction 1
instruction 2
instruction 3
cycle C
cycle C+1
cycle C+2
cycle C+3
cycle C+4

FIG. 13

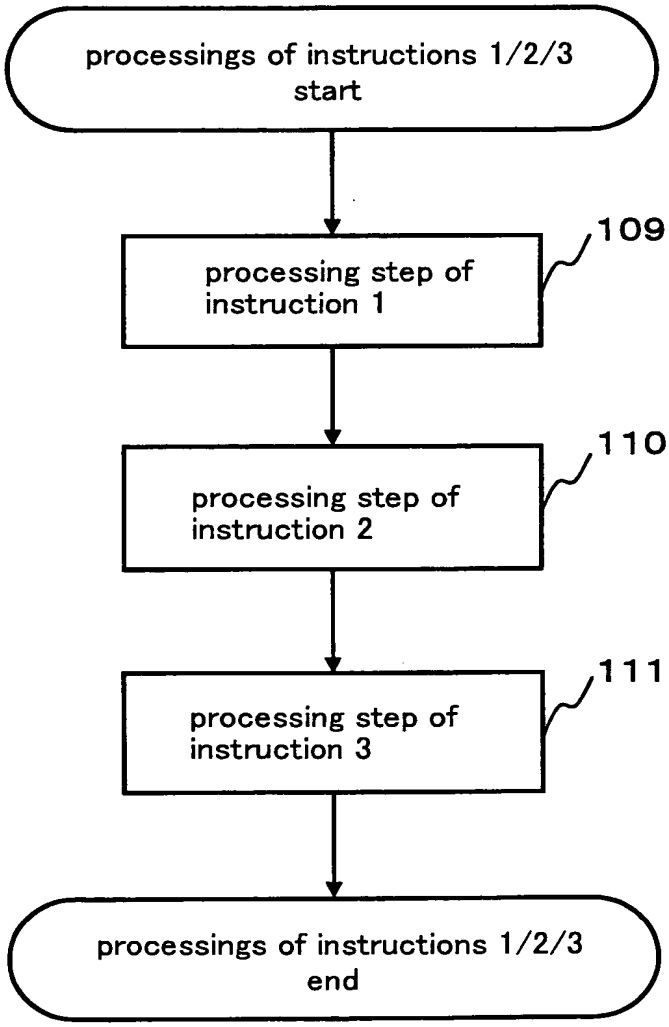

processings of instructions 1/2/3 start
processing step of instruction 1
109
processing step of instruction 2
110
processing step of instruction 3
111
processings of instructions 1/2/3 end

FIG. 14

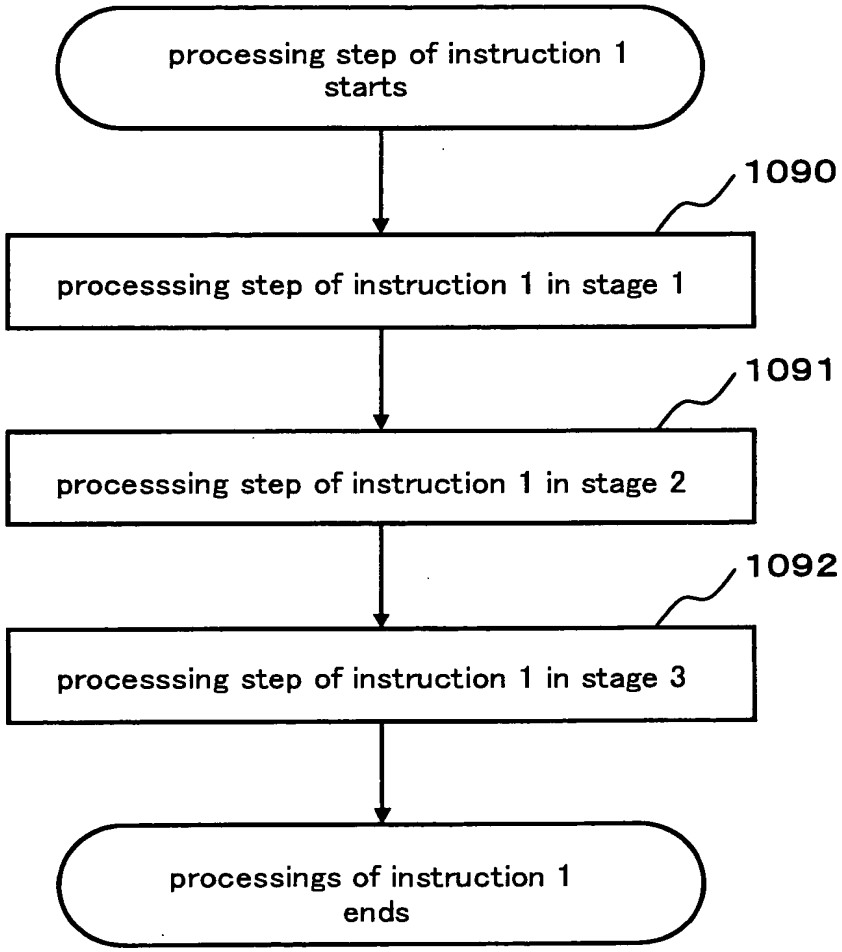

processing step of instruction 1 starts
1090
processsing step of instruction 1 in stage 1
1091
processsing step of instruction 1 in stage 2
1092
processsing step of instruction 1 in stage 3
processings of instruction 1 ends

FIG. 15

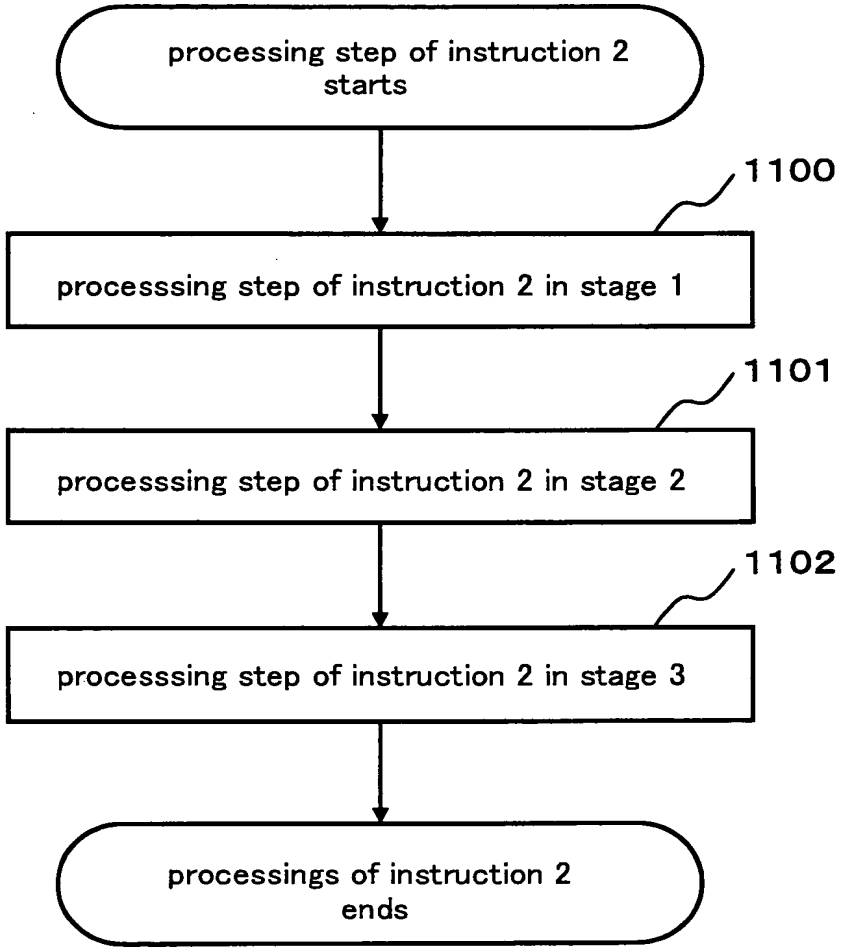

processing step of instruction 2 starts
1100
processsing step of instruction 2 in stage 1
1101
processsing step of instruction 2 in stage 2
1102
processsing step of instruction 2 in stage 3
processings of instruction 2 ends

FIG. 16

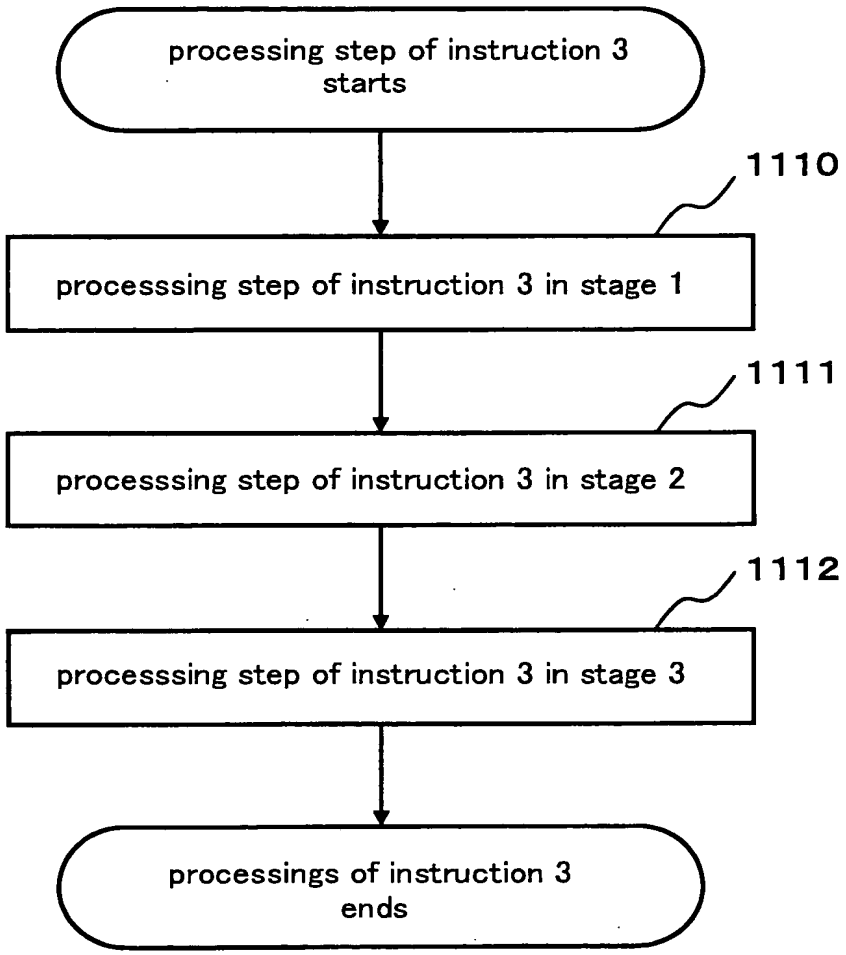

processing step of instruction 3 starts
1110
processsing step of instruction 3 in stage 1
1111
processsing step of instruction 3 in stage 2
1112
processsing step of instruction 3 in stage 3
processings of instruction 3 ends

FIG. 17

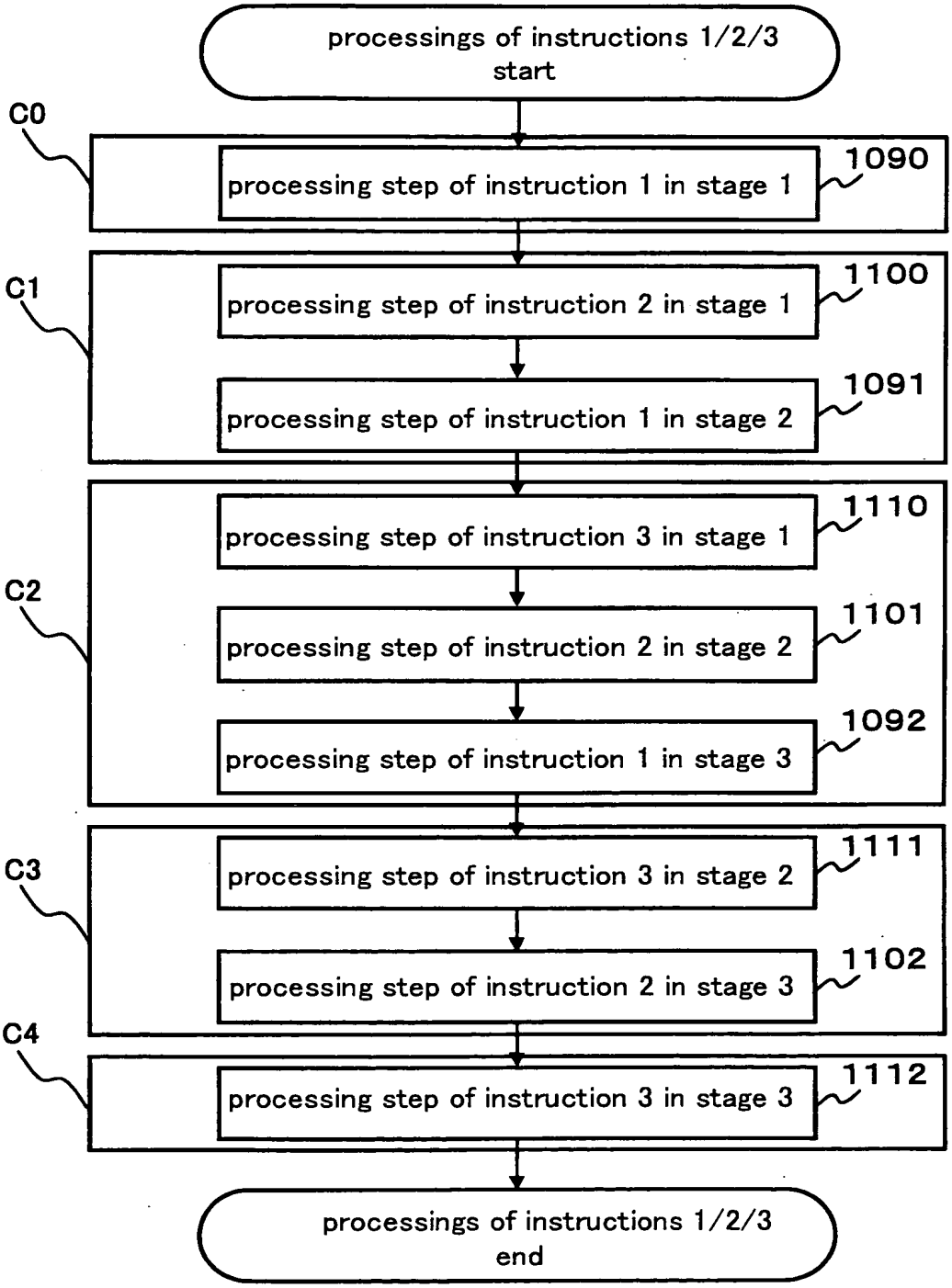

processings of instructions 1/2/3 start
C0
processing step of instruction 1 in stage 1
1090
C1
processing step of instruction 2 in stage 1
1100
processing step of instruction 1 in stage 2
1091
C2
processing step of instruction 3 in stage 1
1110
processing step of instruction 2 in stage 2
1101
processing step of instruction 1 in stage 3
1092
C3
processing step of instruction 3 in stage 2
1111
processing step of instruction 2 in stage 3
1102
C4
processing step of instruction 3 in stage 3
1112
processings of instructions 1/2/3 end

FIG. 18

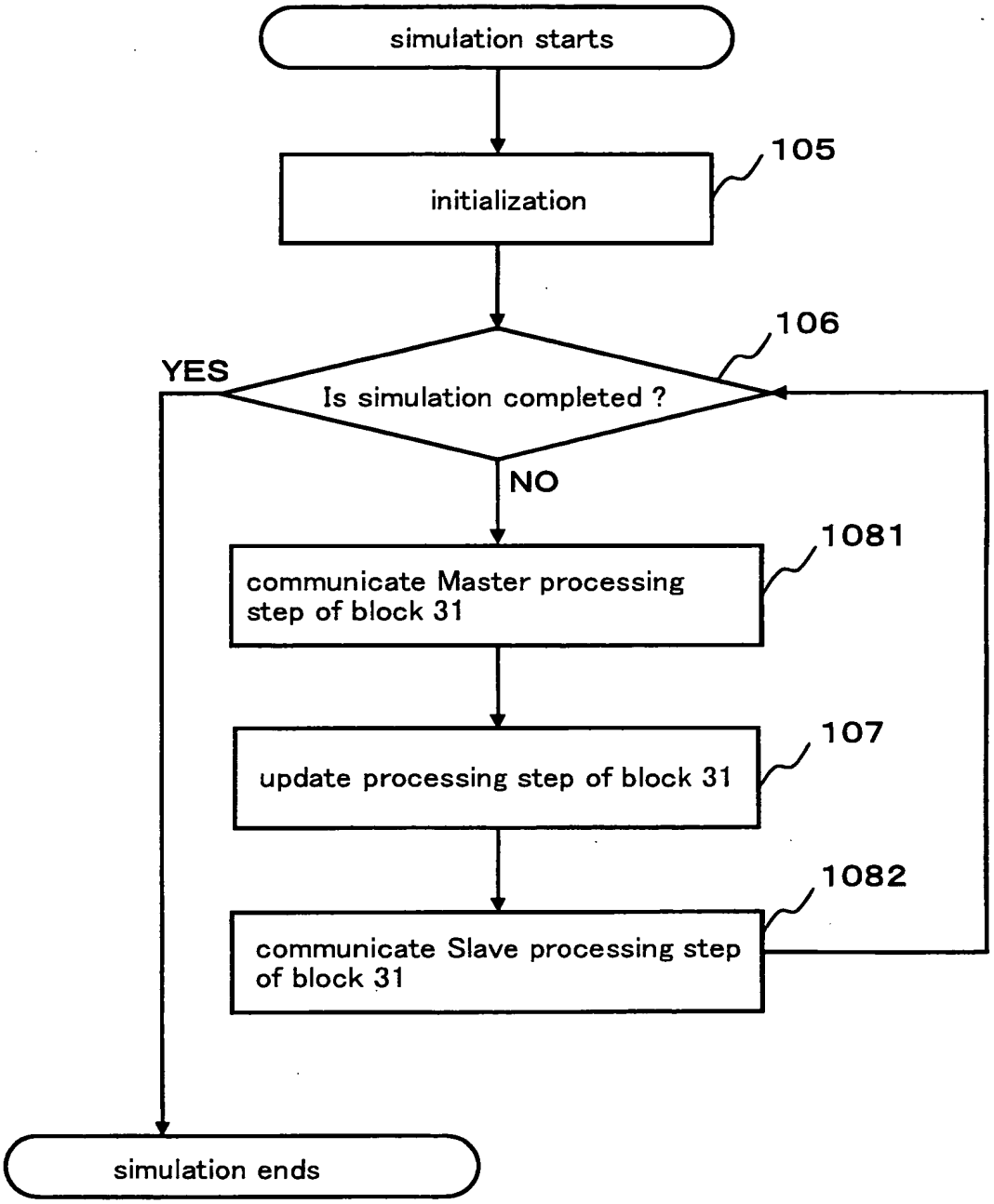
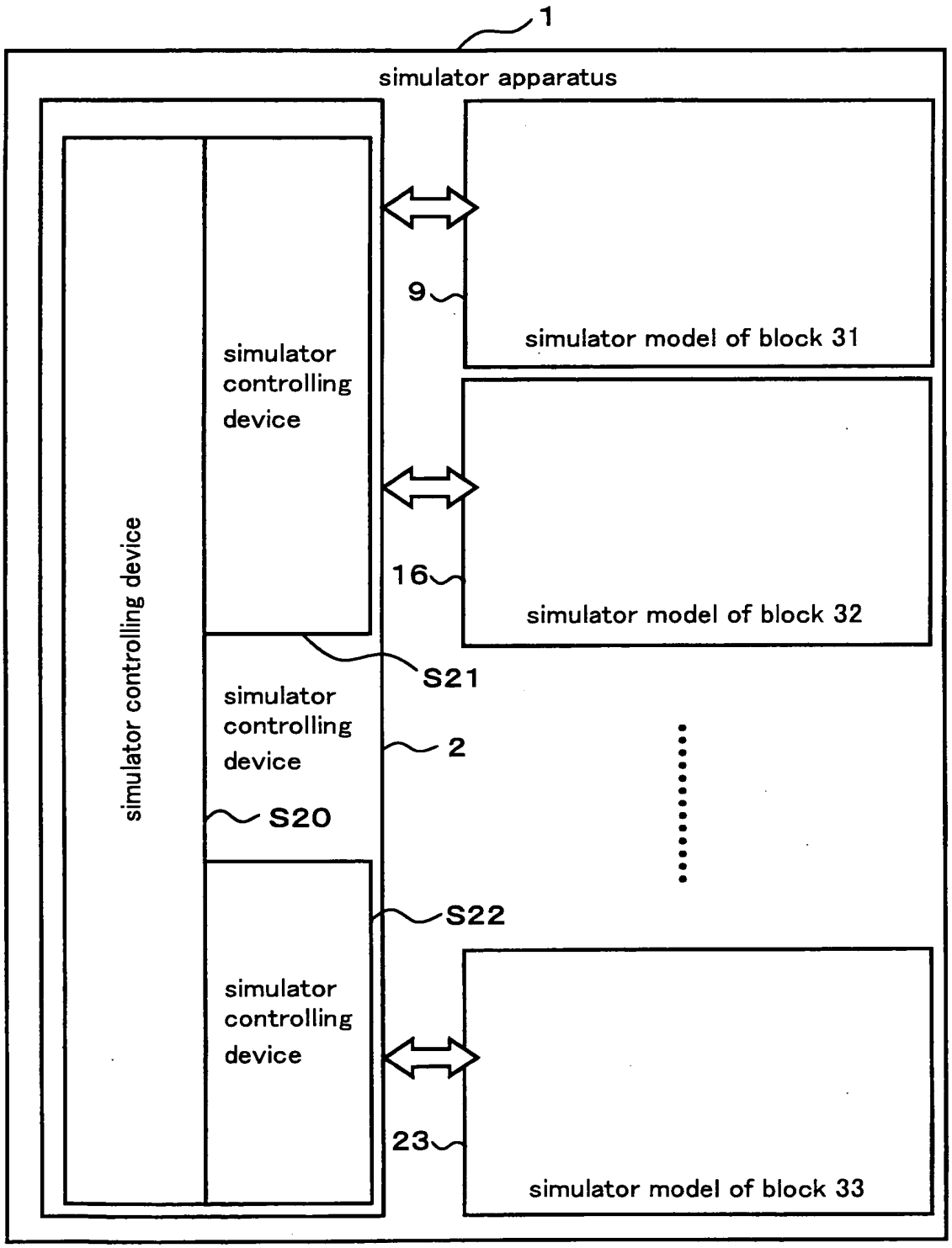

simulation starts
initialization
105
Is simulation completed ?
106
YES
NO
communicate Master processing step of block 31
1081
update processing step of block 31
107
communicate Slave processing step of block 31
1082
simulation ends

FIG. 19


1
simulator apparatus
simulator controlling device
simulator controlling device
9
simulator model of block 31
16
simulator model of block 32
S21
simulator controlling device
2
S20
S22
simulator controlling device
23
simulator model of block 33